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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Kenji Kimura

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11/28/2007

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EXAMINER

DANIELS, ANTHONY J

ART UNIT

PAPER NUMBER

2622

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/715,741	Applicant(s) KIMURA ET AL.	
	Examiner Anthony J. Daniels	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3,6-10,12,13,16 and 19-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3,6-10,12,13,16 and 19-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The amendment, filed 8/30/2007, has been entered and made of record. Claims 3,6-10,12,16 and 19-27 are pending in the application.

Response to Arguments

1. Applicant's arguments with regarding the independent claims and the Hashimoto reference have been considered but are moot in view of the new ground(s) of rejection.

The examiner is still using the Hashimoto reference in rejection. However, a new interpretation of the claims is being made. See rejection below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 3,6,7,9,12,16 and 19-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto (US # 4,910,599).

As to claim 3, Hashimoto teaches an image sensor controller (Figure 10, driver “206”) that controls an image sensor (Figure 9 and 10, CCD “201”; Col. 12, Lines 32-36) having a light receiving section and a transfer section that receives data signals from the light receiving section (Col. 12, Lines 15-19), the image sensor controller comprising: a drive controller (Figure 10,

clock “207”) configured to supply a shift/transfer clock to the transfer section, the shift/transfer clock used for shifting the data signals and transferring the data signals (Col. 12, Lines 34-36), the shift/transfer clock being configured to have a first frequency during a first period in which a first data signal of the data signals is outputted from a dummy pixel of a plurality of pixels included in the light receiving section (Figure 9, pixels of unnecessary region “Va”; Figure 11A, “Tva”; *{The examiner interprets the dummy pixel as a pixel from the unnecessary region “Va”.* *The claim does not require nor does the specification explicitly define the dummy pixel region as a region that is optically black or light-shielded.}*); the shift/transfer clock being configured to have a second frequency during a second period in which a second data signal of the data signals is outputted from a non-reading pixel of the plurality of pixels (Figure 9, pixels of optical black region “OB”; Figure 11A, “Tvob”; *{The examiner interprets the non-reading pixel as a pixel from the optical black region “OB”. The claim does not require nor does the specification explicitly define the non-reading pixel region as a region that is not optically black or light-shielded. The optical black pixels in Hashimoto are not used as image signals.}*); the shift/transfer clock being configured to have a third frequency during a third period in which a third data signal of the data signals is outputted from a reading pixel of the plurality of pixels (Figure 9, pixels of effective region “B”; Figure 11A, “Tvb”); the first frequency being higher than the second frequency; and the second frequency being higher than the third frequency (Figure 11A; $F_{va} > F_{vob} > F_{vb}$).

As to claim 6, Hashimoto teaches an image sensor controller according to claim 3, wherein the drive controller includes a pattern selector configured to select, from among a plurality of clock patterns for setting the shift/transfer clock, a specific clock pattern for each

period during which the data signals are outputted from the transfer section of the image sensor (Figure 11A).

As to claim 7, Hashimoto teaches an image sensor controller according to claim 6, wherein the drive controller includes a memory configured to store the plurality of clock patterns (*It is inherent in the embodiment that there is a memory for storing instructions for setting the clock patterns of Figure 11A.*); and the pattern selector selects from among the plurality of clock patterns stored in the memory a specific clock pattern for each image data output period based on pattern switch timing setting information, and supplies the shift/transfer clock to the transfer section of the image sensor based on the clock pattern selected (Figure 11A).

As to claim 9, Hashimoto teaches an image sensor controller according to claim 3, further comprising: an image processing controller configured to (i) supply an A/D conversion/transfer clock to an A/D converter that converts analog data signals sent from the transfer section of the image sensor to digital data signals, and (ii) receives the digital data signals outputted from the A/D converter based on the supplied A/D conversion/transfer clock, wherein the image processing controller disables an output operation of the A/D converter during periods in which the A/D converter outputs the data signals obtained from the dummy pixel and non-reading pixel (*Neither the unnecessary pixel data nor the optical black pixel data being output by the A/D converter is inherent in the device of Hashimoto. Thus, the output of the A/D converter is disabled from outputting the unnecessary data and the optical black data.*).

As to claim 12, Hashimoto teaches an electronic device (Figure 10), comprising: an image sensor (Figure 10, CCD "201") that has a light receiving section and a transfer section that receives data signals from the light receiving section (Col. 12, Lines 15-19); and an image sensor

controller (Figure 10, driver “206”) configured to control the image sensor (Col. 12, Lines 33-36), the image sensor controller comprising: a drive controller configured to supply a shift/transfer clock to the transfer section, the shift/transfer clock used for shifting the data signals and transferring the data signals (Col. 12, Lines 33-36), the shift/transfer clock being configured to have a first frequency during a first period in which a first data signal of the data signals is outputted from a dummy pixel of a plurality of pixels included in the light receiving section (Figure 9, pixels of unnecessary region “Va”; Figure 11A, “Tva”; *{The examiner interprets the dummy pixel as a pixel from the unnecessary region “Va”. The claim does not require nor does the specification explicitly define the dummy pixel region as a region that is optically black or light-shielded.}*); the shift/transfer clock being configured to have a second frequency during a second period in which a second data signal of the data signals is outputted from a non-reading pixel of the plurality of pixels (Figure 9, pixels of optical black region “OB”; Figure 11A, “Tvob”; *{The examiner interprets the non-reading pixel as a pixel from the optical black region “OB”. The claim does not require nor does the specification explicitly define the non-reading pixel region as a region that is not optically black or light-shielded. The optical black pixels in Hashimoto are not used as image signals.}*); the shift/transfer clock being configured to have a third frequency during a third period in which a third data signal of the data signals is outputted from a reading pixel of the plurality of pixels (Figure 9, pixels of effective region “B”; Figure 11A, “Tvb”); the first frequency being higher than the second frequency; and the second frequency being higher than the third frequency (Figure 11A; $F_{va} > F_{vob} > F_{vb}$).

As to claim 16, Hashimoto teaches a method for controlling an image sensor (Figure 10, CCD “201”) having a light receiving section and a transfer section that receives data signals

from the light receiving section (Col. 12, Lines 15-19), the method comprising: controlling the frequency of a shift/transfer clock for shifting the data signals and transferring the data signals by: setting the frequency of the shift/transfer clock to a first frequency in a dummy pixel output period during which a first data signal obtained from a dummy pixel region is outputted from the transfer section (Figure 9, pixels of unnecessary region "Va"; Figure 11A, "Tva"; *{The examiner interprets the dummy pixel as a pixel from the unnecessary region "Va". The claim does not require nor does the specification explicitly define the dummy pixel region as a region that is optically black or light-shielded.}*), setting the frequency of the shift/transfer clock to a second frequency in a non-reading pixel output period during which a second data signal obtained from a non-reading pixel region is outputted from the transfer section (Figure 9, pixels of optical black region "OB"; Figure 11A, "Tvob"; *{The examiner interprets the non-reading pixel as a pixel from the optical black region "OB". The claim does not require nor does the specification explicitly define the non-reading pixel region as a region that is not optically black or light-shielded. The optical black pixels in Hashimoto are not used as image signals.}*), and setting the frequency of the shift/transfer clock to a third frequency in a reading pixel output period during which a third data signal obtained from a reading pixel region is outputted from the transfer section (Figure 9, pixels of effective region "B"; Figure 11A, "Tvb"); the first frequency being higher than the second frequency; and the second frequency being higher than the third frequency (Figure 11A; $F_{va} > F_{vob} > F_{vb}$); and supplying the shift/transfer clock to the transfer section which shifts and transfers received image data signals based on the frequency of the shift/transfer clock (Col. 12, Lines 33-36).

As to claim 19, Hashimoto teaches a method according to claim 16, further comprising selecting, from among a plurality of clock patterns for setting the shift/transfer clock, a specific clock pattern for each period during which the data signals are outputted from the transfer section of the image sensor (Figure 11A).

As to claim 20, Hashimoto teaches an electronic device according to claim 12, wherein the transfer section transfer the third data signal of the reading pixel region at a first transfer rate, and transfer the second data signal of the non-reading pixel region at a second transfer rate, which is faster than the first transfer rate, and transfer the first data signal of the dummy pixel region at a third transfer rate, which is faster than the second transfer rate (Figure 11A; $F_{va} > F_{vob} > F_{vb}$).

As to claim 21, Hashimoto teaches an image sensor (Figure 9, Figure 10, CCD "201") comprising: a light receiving section; and a transfer section that receives data signals from the light receiving section and transfer the image data signals (Col. 12, Lines 15-19), wherein the transfer section transfer the data signals of a reading pixel region at a first transfer rate (Figure 9, pixels of effective region "B"; Figure 11A, "Tvb"; F_{vb}), and transfer the data signals of a non-reading pixel region at a second transfer rate (Figure 9, pixels of optical black region "OB"; Figure 11A, "Tvob"; *{The examiner interprets the non-reading pixel as a pixel from the optical black region "OB". The claim does not require nor does the specification explicitly define the non-reading pixel region as a region that is not optically black or light-shielded. The optical black pixels in Hashimoto are not used as image signals.}*), which is faster than the first transfer rate (Figure 11A, $F_{vob} > F_{vb}$), and transfer the data signals of a dummy pixel region at a third transfer rate (Figure 9, pixels of unnecessary region "Va"; Figure 11A, "Tva"; *{The examiner*

interprets the dummy pixel as a pixel from the unnecessary region "Va". The claim does not require nor does the specification explicitly define the dummy pixel region as a region that is optically black or light-shielded.}), which is faster than the second transfer rate (Figure 11A, $F_{va} > F_{vob}$).

As to claim 22, Hashimoto teaches an image sensor controller (Figure 10, driver "206") that controls an image sensor (Figure 9 and 10, CCD "201"; Col. 12, Lines 32-36) having a light receiving section and a transfer section that receives data signals from the light receiving section (Col. 12, Lines 15-19), the image sensor controller comprising: a drive controller configured to supply a shift/transfer clock to the transfer section, the shift/transfer clock being used for shifting the data signals and transferring the data signals (Figure 10, clock "207"), the shift/transfer clock being configured to have a first frequency during a first period in which a first data signal of the data signals is outputted from a first pixel of a plurality of pixels included in the light receiving section (Figure 9, pixels of unnecessary region "Va"; Figure 11A, "Tva"; *{The examiner interprets the first pixel as a pixel from the unnecessary region "Va".}*), the shift/transfer clock being configured to have a second frequency during a second period in which a second data signal of the data signals is outputted from a second pixel of the plurality of pixels (Figure 9, pixels of optical black region "OB"; Figure 11A, "Tvob"; *{The examiner interprets the second pixel as a pixel from the optical black region "OB".}*), and the shift/transfer clock being configured to have a third frequency during a third period in which a third data signal of the data signals is outputted from a third pixel of the plurality of pixels (Figure 9, pixels of effective region "B"; Figure 11A, "Tvb"; *{The examiner interprets the third pixel as a pixel from the effective region "B".}*), the first data signal being outputted before the second data signal, the

second data signal being outputted before the third data signal (Figure 11A), the first frequency being higher than the second frequency, and the second frequency being higher than the third frequency (Figure 11A; $F_{va} > F_{vob} > F_{vb}$).

As to claim 23, Hashimoto teaches an image sensor controller according to claim 20 the first pixel being a dummy pixel, the second pixel being a non-reading pixel, and the third pixel being a reading pixel. *See rejection of claim 22 and the rejection of claim 3 concerning the interpretation of the dummy pixel and the non-reading pixel.*

As to claim 24, Hashimoto teaches an image sensor controller (Figure 10, driver “206”) that controls an image sensor (Figure 9 and 10, CCD “201”; Col. 12, Lines 32-36) having a light receiving section and a transfer section that receives data signals from the light receiving section (Col. 12, Lines 15-19), the image sensor controller comprising: a drive controller configured to supply a shift/transfer clock to the transfer section, the shift/transfer clock being used for shifting the data signals and transferring the data signals (Figure 10, clock “207”); the shift/transfer clock being configured to have a first frequency during a first period in which a first data signal of the data signals is outputted from a first pixel of a plurality of pixels that are arranged in one line of the light receiving section (Figure 9, pixels of unnecessary region “Va”; Figure 11A, “Tva”; *{The examiner interprets the first pixel as a pixel from the unnecessary region “Va”. In Figure 9, a line is formed in the unnecessary region “Va” among other pixels.}*); the shift/transfer clock being configured to have a second frequency during a second period in which a second data signal of the data signals is outputted from a second pixel of the plurality of pixels (Figure 9, pixels of optical black region “OB”; Figure 11A, “Tvob”; *{The examiner interprets the second pixel as a pixel from the optical black region “OB”.}*); the shift/transfer clock being configured

to have a third frequency during a third period in which a third data signal of the data signals is outputted from a third pixel of the plurality of pixels (Figure 9, pixels of effective region "B"; Figure 11A, "Tvb"; *{The examiner interprets the third pixel as a pixel from the effective region "B".}*); the first data signal being outputted before the second data signal; the second data signal being outputted before the third data signal (Figure 11A); the first frequency being higher than the second frequency; and the second frequency being higher than the third frequency (Figure 11A; $F_{va} > F_{vob} > F_{vb}$).

As to claim 25, Hashimoto teaches an image sensor controller (Figure 10, driver "206") that controls an image sensor (Figure 9 and 10, CCD "201"; Col. 12, Lines 32-36) having a light receiving section and a transfer section that receives data signals from the light receiving section (Col. 12, Lines 15-19), the image sensor controller comprising: a drive controller configured to supply a transfer clock to the transfer section, the transfer clock being used for transferring the data signals (Figure 10, clock "207"); the transfer clock being configured to have a first frequency during a first period in which a first data signal of the data signals outputted from a first pixel of a plurality of pixels included in the light receiving section is transferred (Figure 9, pixels of unnecessary region "Va"; Figure 11A, "Tva"; *{The examiner interprets the first pixel as a pixel from the unnecessary region "Va".}*); the transfer clock being configured to have a second frequency during a second period in which a second data signal of the data signals outputted from a second pixel of the plurality of pixels is transferred (Figure 9, pixels of optical black region "OB"; Figure 11A, "Tvob"; *{The examiner interprets the second pixel as a pixel from the optical black region "OB".}*); the transfer clock being configured to have a third frequency during a third period in which a third data signal of the data signals outputted from a

third pixel of the plurality of pixels is transferred (Figure 9, pixels of effective region "B"; Figure 11A, "Tvb"; *{The examiner interprets the third pixel as a pixel from the effective region "B".}*); the first frequency being higher than the second frequency (Figure 11A, $F_{va} > F_{vob}$); the first data signal being transferred before the second data signal; the second data signal being transferred before the third data signal (Figure 11A); the first data signal, the second data signal, and the third data signal being transferred during at least a part of a fourth period between a first pulse of a shift signal to a second pulse next to the first pulse of the shift signal (Figures 11A and 11B, shift signal is " Φ_s ";).

As to claim 26, Hashimoto teaches an image sensor controller according to claim 25, wherein the second frequency being higher than the third frequency (Figure 11A, $F_{vob} > F_{vb}$).

As to claim 27, Hashimoto teaches an image sensor controller (Figure 10, driver "206") that controls an image sensor (Figure 9 and 10, CCD "201"; Col. 12, Lines 32-36), the image sensor controller comprising: a drive controller configured to supply a transfer clock and a shift signal to the image sensor, the transfer clock being used for transferring the data signals (Figure 10, clock "207"); the transfer clock being configured to have a first frequency during a first period in which a first data signal of the data signals outputted from a first pixel of a plurality of pixels included in the light receiving section is transferred (Figure 9, pixels of unnecessary region "Va"; Figure 11A, "Tva"; *{The examiner interprets the first pixel as a pixel from the unnecessary region "Va".}*); the transfer clock being configured to have a second frequency during a second period in which a second data signal of the data signals outputted from a second pixel of the plurality of pixels is transferred (Figure 9, pixels of optical black region "OB"; Figure 11A, "Tvob"; *{The examiner interprets the second pixel as a pixel from the optical black*

region "OB".}); the transfer clock being configured to have a third frequency during a third period in which a third data signal of the data signals outputted from a third pixel of the plurality of pixels is transferred (Figure 9, pixels of effective region "B"; Figure 11A, "Tvb"; {The examiner interprets the third pixel as a pixel from the effective region "B".}); the first frequency being higher than the second frequency (Figure 11A, $F_{va} > F_{vob}$); the first data signal being transferred before the second data signal; the second data signal being transferred before the third data signal (Figure 11A); the first data signal, the second data signal, and the third data signal being transferred during at least a part of a fourth period between a first timing that a shift signal changes from a first level to a second level and a second timing that a shift signal changes from the first level to the second level next to the first timing (Figures 11A and 11B, shift signal is " Φ_s ";).

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US # 4,910,599) in view of Hata (US # 6,100,928).

As to claim 8, Hashimoto teaches an image sensor controller according to claim 3, further comprising: an image processing controller configured to (i) supply an A/D conversion/transfer clock to an A/D converter that converts analog data signals sent from the transfer section of the image sensor to digital data signals and (ii) receives the digital data signals outputted from the A/D converter based on the supplied A/D conversion/transfer clock (*A/D conversion circuits are inherent in CCD imaging applications.*); wherein the image processing controller invalidates data signals obtained from dummy pixel (*Dummy pixel data is not included in the effective imaging. Therefore, it is invalidated as image data at some point.*) and the non-reading pixel (Col. 13, Lines 33-58). The claim differs from Hashimoto in that it further requires that the image processing controller invalidates data signals received from A/D converter.

In the same field of endeavor, Hata teaches a digital camera comprising a CCD which outputs image data to an A/D converter before it is input to an image processing device (Figure 1, A/D "106", IPP "107"). In light of the teaching of Hata, it would have been obvious to one of ordinary skill in the art to include the A/D converter before image processing in the system of Hata, because an artisan of ordinary skill in the art would recognize the numerous advantages of digital processing over analog processing.

2. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US # 4,910,599) in view of Kochi (US # 5,191,426).

As to claim 10, Hashimoto teaches an image sensor controller according to claim 1, further comprising: an image processing controller configured to (i) supply an A/D conversion/transfer clock to an A/D converter that converts analog data signals sent from the transfer section of the image sensor to digital data signals and (ii) receives the digital data signals outputted from the A/D converter based on the supplied A/D conversion/transfer clock (*A/D conversion circuits are inherent in CCD imaging applications.*). The claim differs from Hashimoto in that it further requires that the image processing controller supplies the A/D conversion/transfer clock at a constant clock frequency, irrespective of the changes in frequency of the shift/transfer clock.

In the same field of endeavor, Kochi teaches a CCD image pickup device including an A/D converter clocked at a constant timing frequency (Col. 5, Lines 3-7). In light of the teaching of Kochi, it would have been obvious to include a constant timing clock frequency for the A/D converter in Hashimoto, because an artisan of ordinary skill in the art would recognize that this clock could also function as the timing for the effective region of the CCD in Hashimoto (see Kochi, Col. 5, Lines 3-7).

3. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US # 4,910,599) in view of Potucek et al. (US # 5,684,609).

As to claim 13, Hashimoto teaches an electronic device according to claim 12. The claim differs from Hashimoto in that it further requires a carriage on which the image sensor is

mounted; a drive device configured to drive the carriage in a scanning direction; and a servo controller configured to perform servo control on the drive device in accordance with servo control information read by the image sensor from a source.

In the same field of endeavor, Potucek et al. teaches an image scanner which reads effective imaging pixels and dark pixels for FPN reduction (Figure 1; Col. 3, Lines 15-44). In light of the teaching of Potucek et al., it would have been obvious to one of ordinary skill in the art to include the increased image output method in the scanner of Potucek et al., because an artisan of ordinary skill in the art would recognize that this would lead to increased scan rates for the image scanner of Potucek et al. (see Hashimoto, Col. 2, Lines 29-35).

The examiner takes **Official Notice** that image scanners complete with a carriage, drive device and servo control are well known and expected in the art. One of ordinary skill in the art would recognize that these components allow for effective and precise operation of an image scanner.

Conclusion

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AD
11/16/2007



LIN YE
SUPERVISORY PATENT EXAMINER